UNIVERSITY OF LONDON

GOLDSMITHS COLLEGE

B. Sc. Examination 2012

COMPUTING AND INFORMATION SYSTEMS

IS51009B (COMP101)

Data Representation and Architecture Modelling

Duration: 2 **hours** 15 **minutes**

Date and time:

There are five questions in this paper. You should answer no more than THREE questions. Full marks will be awarded for complete answers to a total of THREE questions. Each question carries 25 marks. The marks for each part of a question are indicated at the end of the part in [.] brackets.

There are 75 marks available on this paper.

Electronic calculators must not be programmed prior to the examination. Calculators which display graphics, text or algebraic equations are not allowed.

THIS PAPER MUST NOT BE REMOVED FROM THE EXAMINATION ROOM

QUESTION 1

(1) Consider the positive binary integer represented in twos complement:

0110110110101011

(a) Express this binary number in octal.

(b) Express this binary number in hexadecimal.

(c) Negate the number (i.e. give the twos complement representation of a negative version of the same number) Use the same number of bits in your answer.

(d) Rewrite the result in (c) using 32-bits.

[8 Marks]

(2) The following questions are about the binary representation of single-precision (32-bit) IEEE 754 floating-point numbers.

(a) How many bits are used for each of the sign, exponent and mantissa fields, and their ordering in a 32-bit word?

(b) How is the exponent encoded? How would you represent an exponent of 52?

(c) In general, floating-point numbers are normalised before being encoded. What does this mean for the most significant bit of the mantissa?

[7 Marks]

(3) (a) Give the 32-bit IEEE 754 representation of the floating point number -1.125_{10}.

(b) How would $-\infty$ and the smallest positive number be represented in this 32-bit format?

[10 Marks]

QUESTION 2

(1) Explain the role of the following CPU registers:

- PC
- IR
- MBR
- MAR

[8 Marks]

(2) Explain how temporal and spatial locality principles improve a computer's performance.

[5 Marks]

(3) Suppose we have a memory and a direct-mapped cache with the following characteristics.

- Memory is byte addressable
- Memory addresses are 16 bits (i.e., the total memory size is 216 = 65536 bytes)
- The cache has 8 rows (i.e., 8 cache lines)
- Each cache row (line) holds 16 bytes of data.

(a) Show how the 16 address bits are allocated to the offset (word bits), index (line bits), and tag parts of the address used to reference the cache.

(b) Below is a sequence of four binary memory addresses in the order they are used to reference memory. Assume that the cache is initially empty. For each reference, write down the tag, the index bits and either the words "hit" or "miss" to indicate whether that reference is a hit or a miss.

Memory address	Tag	Index	Hit/Miss
0010 1101 1011 0011			
0000 0110 1111 1100			
0010 1101 1011 1000			
1010 1010 1010 1011			

[12 Marks]

QUESTION 3

(1) (a) Explain the concept of hazards in pipelining.

(b) Briefly explain control hazards.

[7 Marks]

(2) Consider the following sequence of instructions being processed on the pipelined 5-stage RISC processor:

Load R4, 100(R2)

Add R5, R2, R3

Sub R6, R4, R5

(a) Identify all the data dependencies in the above instruction sequence. For each dependency, indicate the two instructions and the register that causes the dependency. Fill in the diagram below to show how this sequence of instructions executes. Show stalls in the schedule, if any, by writing "stall" in that square. The first row for the Load instruction is written for you. How long does it take for the instruction sequence to complete?

Clock Cycle	1	2	3	4	5	6	7	8	9	10	11
Load	IF	ID	EX	MEM	WB						
Add											
Sub											

[11 Marks]

(b) Now, assume that the pipeline used operand forwarding, draw a diagram similar to the above that represents the flow of instructions through the pipeline during each clock cycle. How long does it take for the instruction sequence to complete in this case?

[7 Marks]

QUESTION 4

(1) State with explanation which layer the following protocols belong to:

- TCP
- UDP
- RARP

[6 Marks]

(2) Explain the concept of subnetting in computer networks.

[3 Marks]

(3) Given a host configuration with an IP address 192.168.45.19 and a subnet mask 255.255.255.248 consider the following questions.

(a) What is the subnet address?

(b) What is the host address?

(c) What is the broadcast address?

(d) What is the number of possible hosts and range of host addresses in this subnet?

[12 Marks]

(4) Explain how error control is achieved in the TCP/IP model and state which layer is responsible for this.

[4 Marks]

QUESTION 5

(1) Draw the state diagram of a process from its creation to termination, including all transitions, and briefly elaborate each state and each transition.

[6 Marks]

(2) Describe the differences among short-term, medium-term, and long-term scheduling.

[6 Marks]

(3) Why is it generally correct to favour I/O-bound processes over CPU-bound processes?

[4 Marks]

(4) Explain the difference between I/O programmed, interrupted-driven I/O and direct memory access. Give the advantages/disadvantages of each.

[9 Marks]