UNIVERSITY OF LONDON

GOLDSMITHS COLLEGE

B. Sc. Examination 2011

COMPUTING AND INFORMATION SYSTEMS

IS51009B (COMP101)

Data Representation and Architecture Modeling

Duration: 1 **hour** 30 **minutes**

Date and time:

There are three questions in this paper. Full marks will be awarded for complete answers to all three questions. The marks for each part of a question are indicated at the end of the part in [.] brackets.

Electronic calculators must not be programmed prior to the examination. Calculators which display graphics, text or algebraic equations are not allowed.

THIS PAPER MUST NOT BE REMOVED FROM THE EXAMINATION ROOM

QUESTION 1

(1) Given the following 8 bit unsigned binary integer, 1 0 1 1 0 0 1 1:

(a) Give the corresponding hexadecimal and decimal values.

(b) What would the decimal value be if the above number was represented as an 8 bit signed (twos complement) integer instead?

(c) Specify the range of integers represented in a 32-bit two's complement notation.

[10 Marks]

(2) (a) Represent the negative integer -23 in two's complement notation.

(b) Use the sign extension rule to find the 32-bit two's complement representation of the integer -23.

(c) What advantages has two's complement notation over signed one?

[10 Marks]

(3) Assume we are using the 32-bit IEEE single precision floating point format. The mantissa has 24 bits including the hidden bit. There is one sign bit and there are eight exponent bits.

(a) What decimal floating point number is represented by the following 32 bits? show your workings.

1100 0001 1000 1110 0000 0000 0000 0000

(b) What is the range of positive numbers in this representation? State when positive overflow and underflow occur.

[15 Marks]

QUESTION 2

(1) Explain the role of each of the following CPU registers:

(a) PC

(b) IR

(c) AC

(d) MBR

[8 Marks]

(2) (a) Explain how the cache memory uses temporal and spatial locality of reference to enhance a computer's performance.

(b) Explain the difference between the following two technologies for memory caching: direct mapping memory cache and fully associative memory cache.

[12 Marks]

(4) Suppose you have designed a processor implementation whose five pipeline stages take the following amounts of time: IF=20ns, ID=10ns, EX=20ns, MEM=35ns and WB=10ns.

(a) What is the minimum clock period for which your processor functions properly?

(b) What should be redesigned first to improve this processor's performance?

(c) Assume this processor is redesigned with 50 pipeline stages. Is it true to say that the new processor is 10 times faster than the previous design with 5 pipeline stages? Explain your answer.

[10 Marks]

QUESTION 3

(1) (a) Why is XHTML necessary when most current browsers already render web pages written in HTML?

(b) Cascading Style Sheets (CSS) rules can be used to declare styles for HTML selectors, CLASS selectors or ID selectors. Using examples of each, briefly explain the purpose for each of the three categories of CSS selectors.

[13 Marks]

(2) Given a host configuration with an IP address 192.168.10.17 and a subnet mask 255.255.255.248:

(a) What is the subnet address?

(d) What is the host address?

(c) What is the broadcast address?

(d) What is the number of possible hosts and range of host addresses in this subnet? subnet?

[14 Marks]

(3) Explain how the TCP/IP suite addresses error control and flow control. State which layer is responsible for this.

[8 Marks]